Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application. Below is a new listing of claims showing amendments relative to the previous version of the claims on file.

claim 12 [withdrawn]
claim 13 [withdrawn]
claim 14 [withdrawn]
claim 15 [withdrawn]
claim 16 [withdrawn]
claim 17 [withdrawn]
claim 18 [withdrawn]
claim 19 [withdrawn]
claim 20 [withdrawn]
claim 21 [withdrawn]
claim 22 [withdrawn]
claim 23 [withdrawn]
claim 24 [withdrawn]
claim 25 [withdrawn]
claim 26 [withdrawn]
claim 27 [withdrawn]
claim 28 [withdrawn]
claim 29 [withdrawn]
claim 30 [withdrawn]
claim 31 [withdrawn]
claim 32 [withdrawn]
claim 33 [withdrawn]
claim 34 [withdrawn]
claim 35 [withdrawn]

claim 36 [withdrawn]

Claim 37 [new] The apparatus for a signal-triggered digital memory system device, said apparatus comprising:

a memory controller signal source for generating a digital control signal;

an input receiver located within said memory device, said input receiver receiving said digital signal for said digital circuit and being responsive to triggering induced by said digital signal;

a conducting interface;

a conducting signal path, said conducting signal path being electrically connected to said conducting interface, said conducting interface being electrically connected to said input receiver, said signal path carrying said digital signal thereover; and

wherein said conducting interface is substantially rectangular in planar view and said conducting signal path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of said conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 38 (new) The apparatus according to Claim 37, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 39 (new) The apparatus according to Claim 38, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of the said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

Claim 40 (new) The apparatus according to Claim 39, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 41 (new) The apparatus according to Claim 38, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 42 (new) The apparatus according to Claim 41, further comprising a circuit substrate, wherein said conducting interface and said conducting signal path are located on said circuit substrate.

Claim 43 (new) The apparatus according to Claim 42, wherein said circuit substrate comprises a printed circuit board and wherein said conducting interface is a pad and said conducting signal path is a trace.

Claim 44 (new) The apparatus according to Claim 43, wherein said pad is substantially square in planar view.

Claim 45 (new) The apparatus according to Claim 43, wherein said trace has a width which is 1/5th of a width of said pad to which said trace is connected.

Claim 46 (new) The apparatus according to Claim 43, wherein when said input receiver is mounted to said pad, said trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of said pad to which said trace is connected.

Claim 47 (new) The apparatus according to Claim 43, wherein when said input receiver is mounted to said pad, said pad has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said trace has a width of 4 mils and a thickness of 1.2 mils.

Claim 48 (new) The apparatus according to Claim 42, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

Claim 49 (new) The circuit substrate for a signal-triggered memory device digital circuit, said circuit substrate comprising:

a conducting interface, substantially rectangular in planar view, for electrical connection to an input receiver of the memory device, said input receiver receiving a digital control signal over said digital circuit and being responsive to triggering induced by said digital control signal;

a conducting signal path having a width which is 1/5th of a width of said conducting interface, said conducting signal path being connected to said conducting interface, said signal path carrying said digital control signal thereover; and

wherein said conducting path connected to said conducting interface has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which said path is connected to thereby produce a reduced reflection of said digital control signal at said connection between said conducting interface and said conducting path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 50 (new) The circuit substrate according to Claim 49, wherein said conducting interface is substantially square in planar view.

Claim 51 (new) The circuit substrate according to Claim 49, wherein said conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which said conducting signal path is connected.

Claim 52 (new) The circuit substrate according to Claim 49, wherein when said input receiver is mounted to said conducting interface, said conducting interface has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said conducting signal path has a width of 4 mils and a thickness of 1.2 mils.

Claim 53 (new) The circuit substrate according to Claim 49, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 54 (new) The circuit substrate according to Claim 53, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

Claim 55 (new) The circuit substrate according to Claim 54, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 56 (new) The circuit substrate according to Claim 53, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 57 (new) The circuit substrate according to Claim 56, wherein said circuit substrate comprises a printed circuit board, said conducting interface is a pad and said conducting signal path is a trace.

Claim 58 (new) The circuit substrate according to Claim 57, said circuit substrate further comprising a signal source for generating said digital control signal.

Claim 59 (new) The circuit substrate according to Claim 58, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.